X Band BiCMOS SiGe 0.35 μm Voltage Controlled Oscillator in Parallel and Reflection Topology and External Phase Noise Improvement Solution

W. Wong, G. Cibiel, J.-G. Tartarin, É. Tournier, R. Plana, O. Llopis

LAAS/CNRS 7, avenue du Colonel Roche, 31077 Toulouse Cedex 04

Abstract — **This paper reports the design of two X band voltage controlled oscillator (VCO) implemented in the same ST Microelectronics SiGe BiCMOS technology and using the same active device. One VCO's design is based on a parallel topology while the other one is based on a serial topology. The chips work with a single supply voltage of 3.3 V, and the measured phase noise performance for the feedback VCO is -85 dBc/Hz @ 100 kHz offset with a tuning range of 0.5 GHz and the simulated phase noise for the negative resistance VCO is -92 dBc/Hz @ 100 kHz offset with a tuning range of 1.1 GHz. Finally, an off chip solution is proposed to improve the phase noise performance.**

I. Introduction

Recent advances in MMIC (Microwave Monolithic Integrated Circuit) design open the way to the integration of complex microwave systems on a chip, such as digital frequency synthesizers. These synthesizers make use of a Phase Locked Loop (PLL), in which the most critical microwave element is the VCO. This circuit has to be optimized in term of phase noise and frequency tuning. Heterojunction bipolar transistors (HBT) Si/SiGe/Si have proven to be good candidates for this application [1] [2]. Their low frequency noise performances are better than their GaAs counterpart and their compatibility in a BiCMOS process enables their integration with CMOS digital circuits. This should lead to integrated synthesizers for which the main features would be: high integration level, low cost and low phase noise. The main issue in an oscillator design deals with the choice of the circuit topology. Many configurations are possible to make a transistor oscillate and to tune the oscillation and it is tricky to evaluate which of these topologies will turn out to the best circuit performance, both in term of phase noise and tuning range.

In this paper, the two main configurations for single transistor VCO are studied (parallel and series feedback). Two circuits have been designed, optimized and compared.

Finally, an off chip technique is prepared to improve the phase noise performance.

II. Circuits Design

For the common active device of both circuits, a trade-off has been made between the LF (Low Frequency) noise performance and the required gain to compensate resonator tank losses. The chosen active device is composed of two transistors in parallel. The total emitter area is 40 μm^2.

A- Parallel Feedback VCO

A simplified design schematic is shown in Fig. 1. The core is a common emitter amplifier which input and output are matched using LC circuits to get a high gain performance close to the oscillation frequency. The tunable resonant tank is designed to match the oscillation condition:

$$\underline{S}_{21amp} \cdot \underline{S}_{21reson} = 1 \qquad (1)$$

In order to achieve the phase oscillation condition, a topology involving two inductances is used. The frequency tuning is realized with varactors C_{tune} in series connected with the resonator (L_R, C_R). Also, these devices are in a series and parallel configuration to improve the frequency tuning (see Fig. 2) [3].

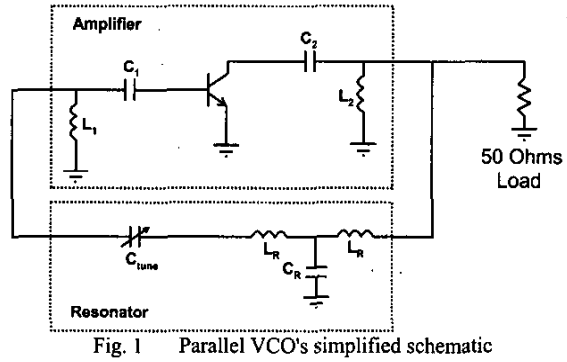

Fig. 1 Parallel VCO's simplified schematic

The inductance's quality factors are optimized by choosing an appropriate geometry to reduce the losses through the substrate and the parasitic coupling capacitor.

0-7803-7694-3/03/$17.00 © 2003 IEEE

An optimum quality factor of 19 has been reached for a 12.7 µm wide line, 2.5 turns spiral inductance.

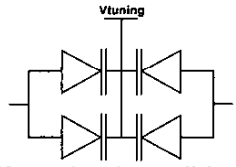

Fig. 2. Varactor's series-parallel configuration

B- Series Feedback VCO

This VCO core consists of a negative resistance amplifier. It is realized through the transistor feedback emitter capacitor C_c. C_c, L_c and C_1, L_1 network values are chosen in order to get the maximum negative resistance at the oscillation frequency.

The VCO tank is composed of an inductor and a varactor for frequency tuning.

The simplified schematic of the series VCO is shown in Fig. 3.

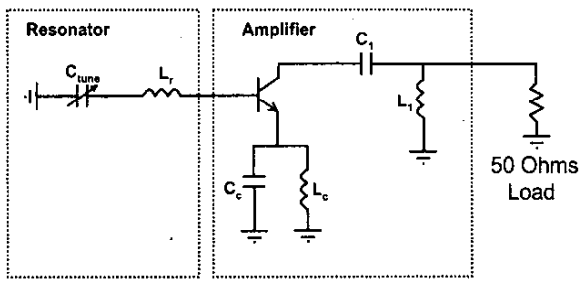

Fig. 3 Serial VCO's simplified schematic

III. Phase Noise Optimization Approach

The oscillator's phase noise close to the carrier is mainly determined by the conversion of the transistor low frequency noise through its nonlinear elements. The two control parameters of the nonlinear elements in a bipolar transistor are the intrinsic voltages Vbe and Vce (base-emitter and collector-emitter).

Any LF fluctuation of one of these two voltages will result in a modulation of the oscillator frequency (and amplitude). It is therefore mandatory to:

1) reduce the global LF noise power leading to these two control voltages
2) reduce the conversion factor with which this LF noise is converted into phase noise.

Previous investigations [4] have demonstrated that the influence on phase noise of the Vbe fluctuations is predominant. Therefore, our main efforts have been dedicated to stabilize this control voltage Vbe.

Reducing the LF noise leading on Vbe is possible using an external filter, as described in section V. But it is also of importance to reduce the base-emitter conversion factor.

In a quasi static perturbation approach of the oscillator nonlinear steady state, this conversion factor may be calculated by the evaluation of the oscillator pushing factor versus the DC value of Vbe. Moreover, the intrinsic voltage Vbe is close to the extrinsic voltage Vbe at low frequencies, which can be chosen for easier calculations. Therefore, our circuit optimization efforts have been dedicated to the reduction of k_p, which is defined as follows:

$$k_p = \frac{\Delta f}{\Delta Vbe} \qquad (2)$$

ΔVbe being a small DC variation of the base-emitter extrinsic voltage and Δf, the resulting oscillator's frequency shift. This approach of phase noise calculation (sometimes known as the modulation approach) is easier and faster than the classical conversion matrices approach, and it is thus well suited for circuit optimization.

The achievement of an oscillation condition around 11-12 GHz is taken in account for parameter values optimization. Thus, the optimum small signal gain has to be obtained at the phase oscillation condition at each parameter (C_{tune}, C_r, L_r, C_c, L_c) value optimization.

Another parameter which has been found to be of importance to reduce k_p is the transistor quiescent point. A high i_{bDC} (and i_{cDC}) current leads to low input impedance at low frequency and to a lower k_p. However, the transistor LF noise often increases with i_{bDC}, but the effect on phase noise of this LF noise increase is weaker than the effect of the conversion coefficient reduction. Therefore, a relatively high bias point has been chosen (I_b=150 µA, I_c=14 mA for feedback VCO and I_b=75 µA, I_c=7 mA for negative resistance VCO) in our oscillator design. In the feedback configuration, higher resonator losses imply higher biasing in order to get higher small signal gain.

IV. Circuit Implementation and Performances

The circuits are realized in ST Microelectronics BiCMOS6G process. A single supply voltage has been planned to bias the circuit at Vcc = 3.3 V, but base and collector biasing (Vb and Vc) have been separated in order to have full liberty to act during measurement. The VCO chips are mounted in a dedicated package for characterization purpose. The block is connected to the ground and represents the ground plane for the external microstrip output RF path. This external path is realized on a 0.254 mm thin Teflon substrate by a thin copper

metallization. To prevent any externally induced LF noise, the VCO is battery biased and coaxial cables are used both for the transistor bias and the VCO tuning voltage. A photograph of the circuit is shown in Fig. 4.

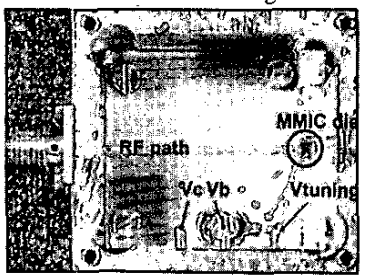

Fig. 4 Mounted VCO chip on a package

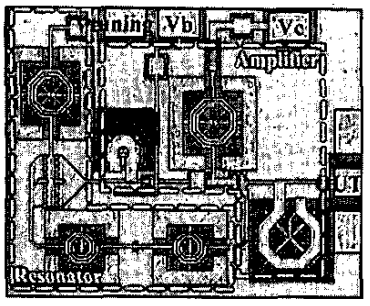

Fig. 5 Microphotograph of the feedback VCO

A- Feedback Voltage Controlled Oscillator

- Simulation

The k_p factor has been optimized at about 1 GHz/V. According to the simulation, the expected performances are a tuning range of 11.4 GHz to 11.9 GHz for a tuning voltage from 0 to 3.6 V. The output power is about -2dBm over the tuning range and the simulated phase noise performance at 100 kHz offset is about -84 dBc/Hz.

- Measurement

A good agreement has been found between simulation and measurement. An oscillation frequency of 11GHz is obtained for a 0 V control voltage and the frequency tuning is about 500MHz wide for a control voltage from 0 to 3.6 V. The output power varies from -2 to -10 dBm over the tuning range. For spectral purity characterization, an home made phase noise measurement set-up has been used. This bench is a delay line discriminator, which uses a cross-correlation technique. This is probably the best suited and easier to implement technique for integrated VCO phase noise evaluation. This technique reaches a noise floor of -145 dBc/Hz at 100kHz offset frequency at X band. The measured parallel VCO phase noise has been found to be about -85 dBc/Hz at 100 kHz offset as shown in Fig. 6 for a 3.3 V bias voltage.

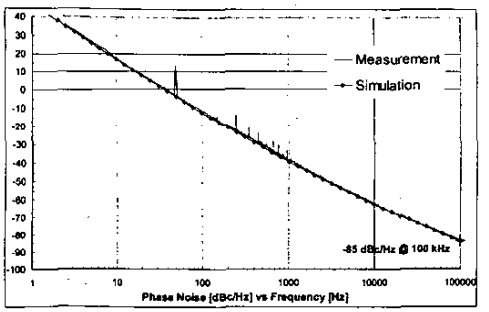

Fig. 6 Measured and simulated phase noise of the feedback VCO at $V_{tuning} = 0$ V

Also, Fig. 7 illustrates the phase noise variation with the transistor bias. Far from the carrier (100 kHz), the improvement of phase noise with a higher biased transistor is obvious. Indeed, the improvement of k_p described in the previous section is probably the reason for this behavior. However, near the carrier (10 Hz), phase noise is not sensitive to this parameter. One might conclude to the fact that LF noise source contribution is different in each case, and that LF noise on the base emitter junction has a strong influence on far from carrier phase noise.

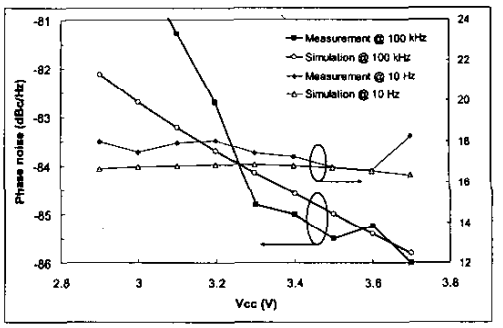

Fig. 7 Measured and simulated phase noise performance at 10Hz and 100 kHz offset versus biasing voltage Vcc, with $I_{bDC} \approx Vcc/R_b$ and $R_b = 14$ kΩ

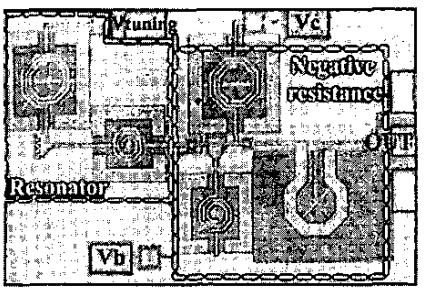

Fig. 8 Microphotograph of the negative resistance VCO

B- Negative Resistance Voltage Controlled Oscillator

- Simulation

Simulation results give an oscillation frequency from 11.3 GHz to 12.4 GHz for a tuning voltage varying from 0 to 3.6 V. The expected output power is about 1 dBm with little variation over the tuning range. The best simulated phase noise is -92 dBc/Hz at 100 kHz offset with a pushing factor of 0.8 GHz/V.

- Measurements

The negative resistance VCO chip has been received very recently, so the measurements will be available at the conference. A comparison with the simulated values will be given in the final version of the paper.

In order to evaluate the phase noise performance of the realized circuits, they are reported on a phase noise MMIC VCO state of the art plot. Our VCO phase noise performances are well located on this plot, and particularly the series feedback one which is among the best published results.

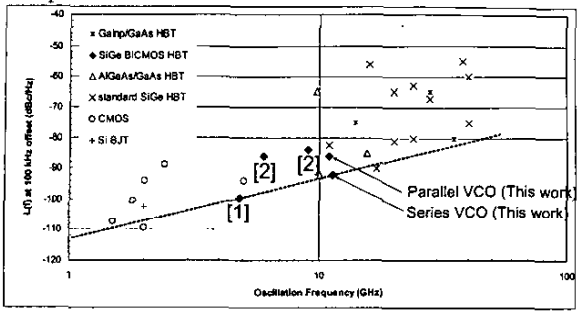

Fig. 9 State of the art of MMIC VCO

V. EXTERNAL SOLUTION TO IMPROVE PHASE NOISE PERFORMANCE

In order to achieve a better phase noise performance, an external solution is proposed to improve VCO spectral purity by an order of several dB. The principle is to reduce phase noise at its origin, i.e. LF noise. In a SiGe HBT, one of the most important LF noise source is the current base-emitter noise. In a monolithic solution, high values inductors are not available as a RF block, and high values resistances are commonly used to bias the base emitter junction. As a consequence, the base emitter current noise is flowing into this resistor, thus creating large fluctuations of the LF voltage Vbe. The proposed solution is the following: a direct access to the transistor base is provided by an external wire bonding. This wire bonding allows the use of a filtering high value capacitance [5] or of a low impedance bias voltage source [6] which stabilizes the extrinsic base emitter voltage at low frequency. This technique has already proven its efficiency on DROs [5, 6] with a typical phase noise improvement of more than 10 dB.

This technique is available on our series VCO circuit. Simulated results already predict a phase noise improvement of 10 dB. Measured results will be given at the conference.

VI. CONCLUSION

Two X band VCO circuits using different topologies have been designed and realized in a silicon BiCMOS process. Our efforts to optimize the circuit performance have been mainly focused towards phase noise. Various attempts have been made to stabilize the low frequency base-emitter voltage fluctuations and their conversion into phase noise. The result is close to the state of the art for the best of the two oscillators, and should be improved by adding to the circuit an external filter.

ACKNOWLEDGEMENT

The authors also wish to acknowledge ST Microelectronics for their support, J. Rayssac and AIME's team for their technical aids.

REFERENCES

[1] H. Jacquinot, J. Majos, P. Senn "5 GHz Monolithic VCO with prescaler using BiCMOS SiGe technology" *Proceedings of the European Microwave Conference September. 2000*

[2] H. Shin, Z. Xu, M. F. Chang "A 1.8 V 6/9 GHz switchable dual band quadrature LC VCO in SiGe BiCMOS technology" *IEEE Radio Frequency Integrated Circuits Symposium* pp. 71-74, June 2002

[3] A. Megej, K. Beilenhoff, and H. L. Hartnagel, "Fully Monolithically integrated feedback voltage controlled oscillator" *IEEE Microwave Guided Wave Letters*, vol. 10, pp. 239-241, June 2000.

[4] O. Llopis, J. M. Dienot, J. Verdier, R. Plana, M. Gayral, J. Graffeuil, " Analytic investigation of frequency sensitivity in microwave oscillators: application to the computation of phase noise in a dielectric resonator oscillator ", *Annals of Telecommunications*, Vol.51, N°3-4, pp.121-129, 1996

[5] M. Régis, O. Llopis, B. Van Haaren, R. Plana, A. Gruhle, J. Rayssac, J. Graffeuil, "Ultra low phase noise C and X band bipolar transistors dielectric resonator oscillators", *IEEE International frequency control symposium 1998*, pp.507-511

[6] G. Cibiel, M. Régis, O. Llopis, V. Giordano, Y. Kersalé, H. Lafontaine, R. Plana, M. Chaubet, "Ultra low phase noise SiGe HBT. Application to a C band sapphire resonator oscillator", *IEEE MTT-Symposium IMS 2002, Seattle USA*, pp. 691-694, June 2002